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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,709	03/03/2004	Satoshi Arai	249946US2	2916

22850 7590 06/19/2008

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
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EXAMINER	
NGUYEN, TUAN HOANG	

ART UNIT	PAPER NUMBER
2618	

NOTIFICATION DATE	DELIVERY MODE
06/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/790,709	ARAI, SATOSHI	
	Examiner	Art Unit	
	TUAN H. NGUYEN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *9-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 11/27/2007 and 03/19/2008 has been considered by Examiner and made of record in the application file.

Response to Arguments

2. Applicant's arguments, see applicant's remarks, filed on 03/03/2008, with respect to the rejection(s) of claims 1-8 under 35 U.S.C § 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hikita et al. (US PAT. 4,792,939 hereinafter, "Hikita") in view of Tomura et al. (U.S PAT. 5,150,282 hereinafter, "Tomura") and further in view of Weber (U.S PAT. 5,335,147).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US PAT. 4,792,939 hereinafter, "Hikita") in view of Tomura et al. (U.S PAT. 5,150,282 hereinafter, "Tomura") and further in view of Weber (U.S PAT. 5,335,147).

Consider claim 1, Hikita teaches a wireless communication apparatus, comprising: a mounting substrate including: a duplexer connected to an antenna terminal (col. 2 lines 25-35); a receiving amplifier and a transmitting amplifier individually connected to the duplexer (col. 3 lines 47-63); a processor unit having a receiving processor and a transmitting processor respectively connected to the receiving and transmitting amplifiers in a region spaced from the receiving and transmitting amplifiers (col. 3 line 63 through col. 4 line 4); and a baseband processor connected to the processor unit (col. 3 lines 47-63); a shield case configured to cover the receiving amplifier, the transmitting amplifier, and the processor unit (col. 8 line 67 through col. 9 line 2).

Hikita does not explicitly show that a shield partition of a conductor provided in contact with the shield case, including, a first partition provided from a top panel of the shield case to a surface of the mounting substrate so as to separate the receiving and transmitting amplifiers by extending from an end of the shield case, and a second partition provided from the top panel to the surface of the mounting substrate by extending from another end of the shield case so as to face the first partition across the processor unit; and a cut, provided from the top panel in the shield case so as to overlay the processor unit between the first and second partitions.

In the same field of endeavor, Tomura teaches a shield partition of a conductor provided in contact with the shield case, including, a first partition provided from a top panel of the shield case to a surface of the mounting substrate so as to separate the receiving and transmitting amplifiers by extending from an end of the shield case (figs. 3-4, items 28, 29 and 30 col. 3 lines 20-58), and a second partition provided from the top panel (24) to the surface of the mounting substrate (21) by extending from another end of the shield case so as to face the first partition across the processor unit (figs. 3-4 col. 3 line 44 through col. 4 line 10); and a cut (as shown in fig. 3 between two grooves of the ribs 28 of the rear casing 24), provided from the top panel in the shield case so as to overlay the processor unit between the first and second partitions (figs. 3-4 col. 3 line 44 through col. 4 line 10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, a shield partition of a conductor provided in contact with the shield case, including, a first partition provided from a top panel of the shield case to a surface of the mounting substrate so as to separate the receiving and transmitting amplifiers by extending from an end of the shield case, and a second partition provided from the top panel to the surface of the mounting substrate by extending from another end of the shield case so as to face the first partition across the processor unit; and a cut, provided from the top panel in the shield case so as to overlay the processor unit between the first and second partitions, as taught by Tomura, in order to provide a shielding structure for high-frequency circuit arrangements capable of electromagnetically shielding each high-frequency functional circuit in a narrow space.

Hikita and Tomura, in combination, fail to teach a cut, provided from the top panel in the shield case so as to overlay the processor unit between the first and second partitions.

However, Weber teaches a cut, provided from the top panel in the shield case so as to overlay the processor unit between the first and second partitions (col. 6 line 57 through col. 7 line 23).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Weber into view of Hikita and Tomura, in order to provide a shielding apparatus for electronic circuitry on a printed circuit board that allows solderless installation of an EMI shield to produce an electronics module that has a high degree of EMI shielding and that permits extensive communication of desired electromagnetic radio frequency and electrical signals by exposing from out of the EMI shield certain portions of the printed circuit board.

Consider claim 2, Hikita further teaches the processor unit monolithically integrates the receiving and transmitting processors and a ground region placed between the receiving and transmitting processors on a semiconductor chip (fig. 9 col. 9 lines 3-13).

Consider claim 3, Tomura further teaches the first partition is connected to a first ground terminal of the processor unit, the first ground terminal being connected to an end of the ground region and being provided in a vicinity of the first partition (col. 3 lines

59-68).

Consider claim 4, Tomura further teaches the second partition is connected to a second ground terminal of the processor unit, the second ground terminal being connected to other end of the ground region and being provided in a vicinity of the second partition (col. 3 lines 59-68).

Consider claim 5, Tomura further teaches at least a part of the respective first and second ground terminals are placed to face each other (col. 3 lines 44-58).

Consider claim 6, Tomura further teaches the shield case is connected to third ground terminals of the processor unit, the third ground terminals being connected to a receiving side ground region and a transmitting side ground region, respectively, of the receiving and transmitting processors provided on opposite ends of the semiconductor chip (col. 3 lines 54-58).

Consider claim 7, Tomura further teaches a conductive member is placed between the cut and a package of the processor unit in contact with the cut and the package (col. 3 lines 44-58).

Consider claim 8, Tomura further teaches an external ground electrode connected to at least one of the first and second ground terminals is provided on a

surface of the package, the surface being in contact with the conductive member (col. 3 lines 47-54).

Conclusion

5. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571)272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571)272-7882882. The fax phone

number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information Consider the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan Nguyen/
Examiner
Art Unit 2618

/Nay A. Maung/
Supervisory Patent Examiner, Art Unit 2618